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10/773,961	02/06/2004	Chia-Te Wu	021653-003500US	7323

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EXAMINER	
RICHARDS, N DREW	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 01/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/773,961	Applicant(s) WU ET AL.	
	Examiner N. Drew Richards	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/1/05 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 3 and 5-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. as applied to claims 1, 6, 8 and 9 above.

With regard to claim 1, Chang et al. discloses an EEPROM integrated circuit structure in figures 1-3 comprising:

a substrate 11 including a surface region 12, the surface region being provided within a first cell region 10;

a gate dielectric layer 26 of a first thickness overlying the surface region 12 of the substrate 11;

a select gate 36 overlying a first portion of the gate dielectric layer 26;

a floating gate 22 overlying a second portion of the gate dielectric layer 26 and coupled to the select gate 36 (coupled through the substrate);

an insulating layer 38 overlying the floating gate 22;

a control gate 24 overlying the insulating layer 38 and coupled to the floating gate 22; and

a tunnel window 32 provided in a stripe configuration, the stripe configuration is disposed within a portion of the gate dielectric layer 26, the portion of the gate dielectric layer being of a second thickness less than the first thickness,

wherein the stripe configuration extending across an entire length of the first cell region from a first field isolation oxide region 14 to a second field isolation oxide region 14 (best seen in figure 3);

Chang et al. teach the stripe configuration in each cell but only explicitly disclose one cell. Thus, Chang et al. do not explicitly teach the stripe extending through the first cell region as well as N other cell regions, N being greater than 2. Official Notice is taken that it would have been obvious to one of ordinary skill in the art at the time of the invention to form an array of EEPROM cells, each cell being formed as taught by Chang et al. It would have been obvious to repeat the cell of Chang et al. in an array to allow a large quantity of bits to be stored. In forming an array of such cells, the stripe 28 would extend through a plurality of cells in a dashed pattern. Since Chang et al. teach their cell being surrounded by isolation region 14 (which is a well known form of FOX region, namely LOCOS) each cell in an array would obviously be separated by a field oxide

region and the stripe configuration would obviously extend (as a dashed pattern) through N other cell regions, N being greater than 2.

With regard to claim 3, Chang et al. do not explicitly teach the width of the tunnel window.

With regard to claim 5, Chang et al. do not explicitly teach the floating gate having a width of 1.5 microns.

Nonetheless, these claimed dimensions are considered obvious to one of ordinary skill in the art in view of Chang et al. One of ordinary skill in the art is motivated to form device features as small as possible to allow as many devices as possible to be formed simultaneously on a single wafer, thus saving of processing costs per device. It would have been obvious to form the tunnel window to a width of less than 0.25 microns to allow the device to be formed as small as possible. It would have been obvious to form the floating gate to a width of 1.5 microns to form the device to a minimal size to allow for greater packing of devices on the chip.

These claims are prima facie obvious without showing that the claimed ranges achieve unexpected results relative to the prior art range. In re Woodruff, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also In re Huang, 40 USPQ2d 1685, 1688(Fed. Cir. 1996)(claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also In re Boesch, 205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and In re Aller, 105 USPQ 233

(CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious).

With regard to claim 6, the limitation of the tunnel window being provided by a phase shift mask is a product-by-process limitation. This product-by-process limitation does not structurally distinguish over the prior art and thus the claim is anticipated by Chang et al.

With regard to claim 7, Chang et al. teach the stripe configuration in each cell but only explicitly disclose one cell. Thus, Chang et al. do not explicitly teach the stripe extending through a plurality of cells each cell being separated by a field oxide region. Official Notice is taken that it would have been obvious to one of ordinary skill in the art at the time of the invention to form an array of EEPROM cells, each cell being formed as taught by Chang et al. It would have been obvious to repeat the cell of Chang et al. in an array to allow a large quantity of bits to be stored. In forming an array of such cells, the stripe 28 would extend through a plurality of cells in a dashed pattern. Since Chang et al. teach their cell being surrounded by isolation region 14 (which is a well known form of FOX region, namely LOCOS) each cell in an array would obviously be separated by a field oxide region.

With regard to claim 8, the substrate is a semiconductor wafer.

With regard to claim 9, the select gate 36, floating gate 22 and control gate 24 are provided within the first cell region and the first cell region is provided within an isolation region 14 (as seen in figure 1 isolation 14 surrounds the active devices).

With regard to claim 10, it would have been further obvious to form an array (as discussed with regard to claim 7 above) with at least 3 rows and 3 columns with that the stripe configuration would extend through other cell regions numbered from 2 through N, where N is an integer greater than 2. It would have been obvious to form such an array to allow a great number of bits to be stored.

4. Claims 2 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. as applied to claims 1, 6, 8 and 9 above, and further in view of Hart et al. (U.S. Patent No. 5,293,331).

With regard to claim 2, Chang et al. is silent as to what material the gate dielectric layer is comprised of.

With regard to claim 4, Chang et al. is silent as to what material comprises the insulating layer between the floating gate and the control gate.

The use of silicon dioxide as a gate dielectric and ONO as the insulating layer between a floating and control gate is well known in the art. These materials are commonly and conventionally used in the semiconductor art. For example, see Hart et al. which teach the use of these materials as a gate dielectric and integrate insulator (insulator between floating and control gates). It would have been obvious to use these commonly used materials for their commonly used purpose. Thus, these claims are considered obvious. The use of conventional materials to perform their known functions in a conventional process is obvious. *In re Raner* 134 USPQ 343 (CCPA 1962).

5. Claims 11-15 and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hart et al. (U.S. Patent No. 5,293,331) in view of D'Arrigo et al. (U.S. Patent No. 5,168,335).

Hart et al. teach a method of manufacturing an EEPROM integrated circuit structure comprising:

providing a substrate 10 including a surface region (figure 7; the surface region is considered to be the region between the left and right FOX1), the surface region being provided within a first cell region (the region shown in figure 7 is considered the first cell region);

forming a gate dielectric layer 22 of a first thickness overlying the surface region of the substrate 10 (figure 7);

patterning the gate dielectric to form a plurality of stripes 24, each of the plurality of stripes 24 being characterized by a second thickness, the second thickness being less than the first thickness (one stripe shown in figure 7; the cell of figure 7 is repeated in the array of figure 10 which shows a plurality of stripes labeled "tunnel oxide stripe"; as seen in figure 7 the stripe 24 has a thickness less than that of gate dielectric 22), each of the plurality of stripes 24 having a predetermined width and a predetermined length (each stripe has a width and length, no patentable weight is given to "predetermined" as the term does not further structurally limit the length or width), at least one of the plurality of stripes 24 includes a portion traversing a portion of the first cell region and other cell regions (as seen in figure 10, tunnel oxide stripe extends through and across cell A and C);

forming a floating gate 26 overlying a portion of the gate dielectric layer 22, the portion of the gate dielectric including the stripe portion 24 traversing through the portion of the gate dielectric layer (the floating gate 26 overlies the portion of gate dielectric 22 where the stripe 24 traverses through it; figure 7);

forming an insulating layer 28 overlying the floating gate (figure 7); and

forming a control gate 30 overlying the insulating layer 28 and coupled to the floating gate (figure 7, the control gate 30 is coupled to the floating gate 26 through the insulating layer 28);

wherein the stripe portion 24 includes a tunnel window for a memory device (the crossing of the floating gate 26 and the stripe 24 is the tunnel window, the device is a memory device; figure 7).

Hart et al. further teach the stripe portion traversing across an entire length of the first cell region but do not teach the stripe traversing from a first field isolation oxide region to a second field isolation oxide region.

D'Arrigo et al. teach an EEPROM in figures 7 and 8, for example. D'Arrigo et al. teach a device having a floating gate 46a,46b and a control gate 62 with a tunnel window 40a in the gate insulating layer beneath the floating gate. D'Arrigo et al. teach an array of such devices in figure 8 and teaches that each cell is isolated from all adjacent cells by field oxide regions 24, 84 and 86.

Hart et al. and D'Arrigo et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to isolate each cell by a field oxide region. The motivation for

doing so is to provide proper deice isolation so that each cell can be addressed, read, or written singly and without causing substrate conduction that could effect an adjacent cell. In combining the continuous stripe portion of Hart et al. with the isolation scheme of D'Arrigo, the stripe would traverse an entire length of the first cell region from a first field isolation oxide region to a second field isolation oxide region. Therefore, it would have been obvious to combine Hart et al. with D'Arrigo et al. to obtain the invention of claim 11.

With regard to claim 12, Hart et al. teach the gate dielectric being a gate oxide but does not explicitly state that the gate oxide is silicon dioxide. Nonetheless, this limitation is implicitly disclosed as Hart et al. teach forming the gate oxide by thermal oxidation of the silicon substrate which is known to produce silicon dioxide.

With regard to claim 14, the insulating layer 28 is an ONO layer coupled between the floating gate and the control gate (figure 7; column 6 lines 38-40).

With regard to claim 17, the at least one of the plurality of stripes of Hart et al. extends through a plurality of cells. In combination with D'Arrigo each of the cells is separated by a field oxide region.

With regard to claim 18, though not explicitly stated, it is nonetheless implicitly understood in the art of semiconductor that the substrate is a semiconductor wafer.

With regard to claim 19, the floating gate and control gate are provided within a cell region which is provided within an isolation region (figures 7 and 8 show the floating gate and control gate in the cell region between isolation regions FOX1).

With regard to claim 13, Hart et al. do not explicitly teach the width of the tunnel window.

With regard to claim 15, the "design width" is being interpreted to be the final width of the floating gate in the final product. Hart et al. do not explicitly teach the floating gate having a width of 1.5 microns.

Nonetheless, these claimed dimensions are considered obvious to one of ordinary skill in the art in view of Hart et al. One of ordinary skill in the art is motivated to form device features as small as possible to allow as many devices as possible to be formed simultaneously on a single wafer, thus saving of processing costs per device. It would have been obvious to form the tunnel window to a width of less than 0.25 microns to allow the device to be formed as small as possible. It would have been obvious to form the floating gate to a width of 1.5 microns to form the device to a minimal size to allow for greater packing of devices on the chip.

These claims are prima facie obvious without showing that the claimed ranges achieve unexpected results relative to the prior art range. In re Woodruff, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also In re Huang, 40 USPQ2d 1685, 1688(Fed. Cir. 1996)(claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also In re Boesch, 205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and In re Aller, 105 USPQ 233

(CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious).

With regard to claim 20, Hart et al. teach an array of their EEPROM cells. For example, figure 10 shows four cells in a 2x2 array. The stripe configuration of Hart et al. runs through the first cell (A) to a second cell (C). However, Hart et al. do not explicitly teach the stripe running through other cell regions numbered from 2 through N, where N is an integer greater than 2 (i.e. Hart et al. figure 10 only shows the tunnel oxide stripe running through 2 cells A and C, but the claim requires a minimum of three cells). Official Notice is taken that it would have been obvious to one of ordinary skill in the art at the time of the invention to form the array of Hart et al. figure 10 to a size much greater than 2x2. It would have been obvious to form the array to a size greater than 2x2 (i.e. including at least 3 cells in each row and column such that each tunnel oxide stripe runs through at least 3 cells) to allow the array to hold a greater number of bits of data. It is well known in the art to form memory chips to hold megabits or more of information so that greater storage can be achieved in each chip. Thus, it would have been obvious to one of ordinary skill in the art to form the tunnel oxide stripe of Hart et al. running across many cells.

6. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hart et al. with D'Arrigo et al. as applied to claims 11-15 and 17-20 above, and further in view of Tanaka et al. (U.S. Patent No. 6,645,856 B2).

Hart et al. with D'Arrigo et al. do not teach the tunnel window being provided using a phase shift mask.

Tanaka et al. teach using a phase shift mask in patterning processes for manufacturing semiconductor devices. See the abstract, for example.

Hart et al. with D'Arrigo et al. and Tanaka et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to one of ordinary skill in the art to use the phase shift mask and technique of Tanaka et al. in forming the tunnel window of Hart et al. The motivation for doing so is to improve the accuracy of dimensions of the pattern transferred to the wafer. Therefore, it would have been obvious to combine Hart et al. and D'Arrigo et al. with Tanaka et al. to obtain the invention of claim 16.

Response to Arguments

7. Applicant's arguments filed 12/1/05 have been fully considered but they are not persuasive.

Applicant has argued that Chang does not teach the stripe configuration extending to other cell regions as recited in claim 1. This is not persuasive. Chang explicitly depicts only a single EEPROM cell in their figures but discusses in column 1 lines 15-20 that an EEPROM device has a plurality of EEPROM cells. One of ordinary skill in the art would recognize that it is readily obvious that the single cell of Chang is formed numerous times in a memory device. With the device of Chang's figures formed

multiple times, the stripe configuration would indeed extend across other cell regions. The stripe configuration may not be a seen as a solid line and may instead be seen as a dashed line. However, the language of the claims do not preclude the stripe configuration being a dashed line across the plurality of cells.

Applicant has also argued that D'Arrigo does not teach the tunnel oxide window extending across the field oxide regions. This is not persuasive as D'Arrigo alone was not relied upon for this teaching. D'Arrigo was relied upon to teach field oxide regions extending around each cell to isolate each cell from adjacent cells. Hart taught the tunnel oxide window extending completely across adjacent tunnel oxide window. In combination with D'Arrigo (which teaches field oxide regions isolating adjacent cells), the tunnel oxide window of Hart would extend across the field oxide regions since Hart teaches a continuous tunnel oxide window across multiple cells.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (571) 272-1736. The examiner can normally be reached on Monday-Friday 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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